



AI Agent:

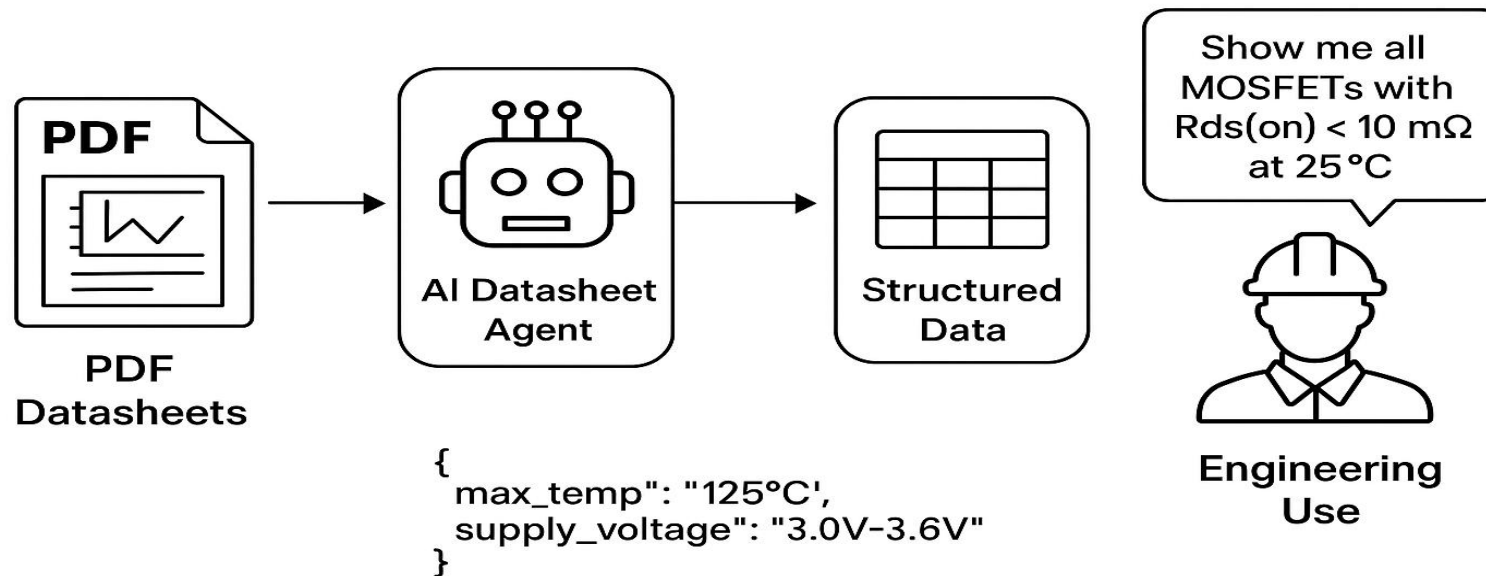
**The Next Stop for Electronic
Design Efficiency Revolution**

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Why we need AI Agent in Datasheet Management ?

AI Agent for Datasheet Management



AI Agents transform datasheets from static PDFs into live, queryable knowledge systems.

PDF to Ontology-Based Content Modeling

- 1) **Classes:** Define microcontroller, processor, memory, package, pin, electrical parameters;
- 2) **Object Properties:** Describe relationships between components (e.g., hasProcessor, hasPin);
- 3) **Data Properties:** Store specific values (e.g., voltage range, Flash capacity, pin name).

Automatic Ontology Construction



ads124s08.
pdf

Class Hierarchy(类层次结构)

- └-- Application (应用类)
 - └-- Application_IndustrialAnalogInput
 - └-- Application_RTDMMeasurement
- └-- CoreDevice (核心器件类)
 - └-- CoreDevice_ADS124S06
 - └-- **CoreDevice_ADS124S08**
- └-- FunctionalModule (功能模块类)
 - └-- FunctionalModule_DeltaSigmaADC
 - └-- FunctionalModule_IDAC
 - └-- FunctionalModule_PGA
 - └-- FunctionalModule_Reference
- └-- OrderablePart (可订购型号类)
 - └-- OrderablePart_ADS124S06IPBS
 - └-- OrderablePart_ADS124S08IPBS
 - └-- **OrderablePart_ADS124S08IRHBR**
- └-- Package (封装类)
 - └-- Package_TQFP_PBS
 - └-- **Package_VQFN_RHB**
- └-- Pin (管脚类)
 - └-- Pin_AnalogInput
 - └-- Pin_AnalogOutput
 - └-- Pin_DigitalControl
 - └-- Pin_GPIO
 - └-- Pin_Power

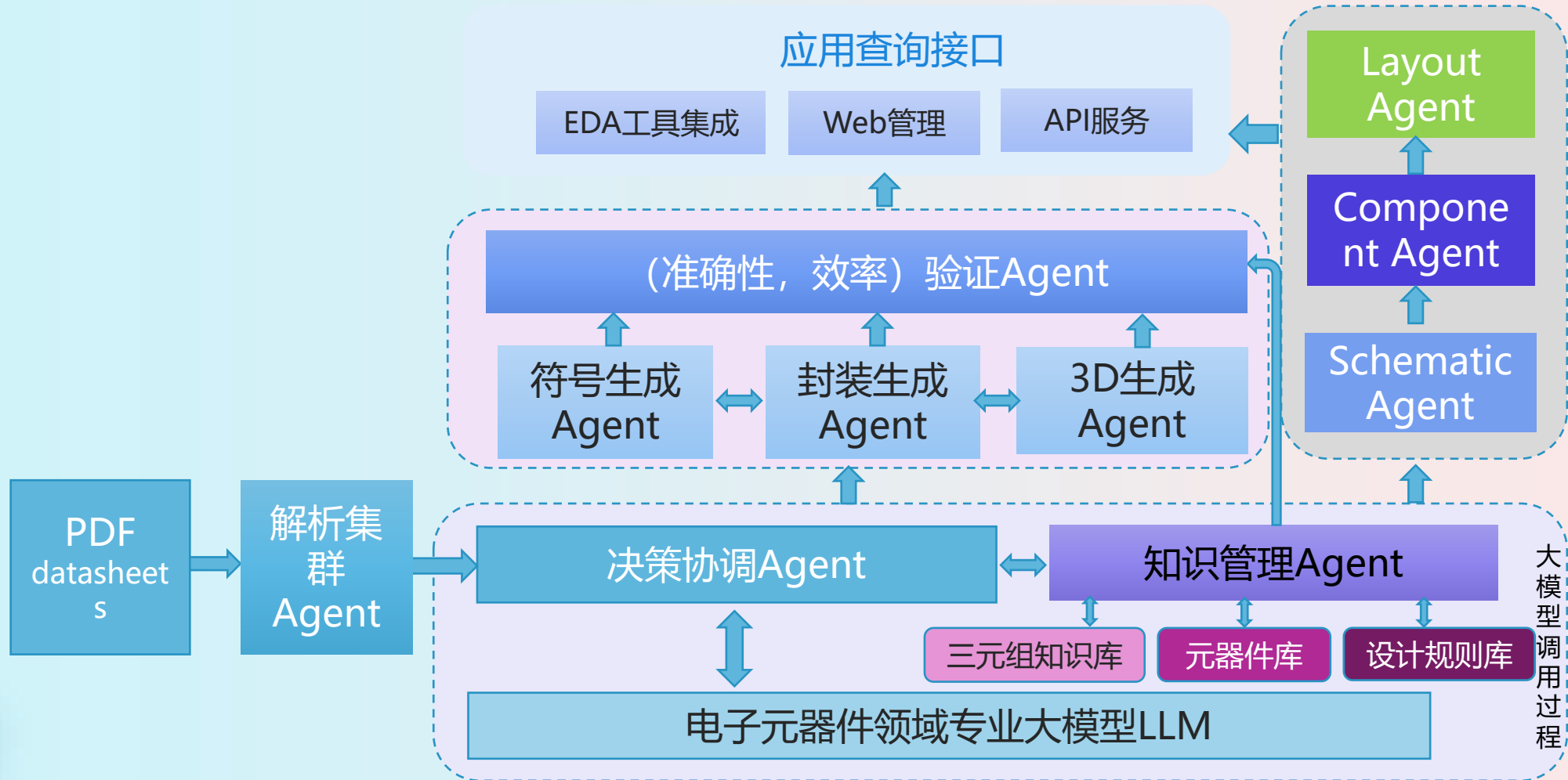
Object Properties(对象属性关系)

- └-- OrderablePart → 关联器件 → CoreDevice
- └-- CoreDevice → 具有封装类型 → Package
- └-- CoreDevice → 包含功能模块 → FunctionalModule
- └-- Pin → 属于器件 → CoreDevice
- └-- CoreDevice → 适用于应用场景 → Application

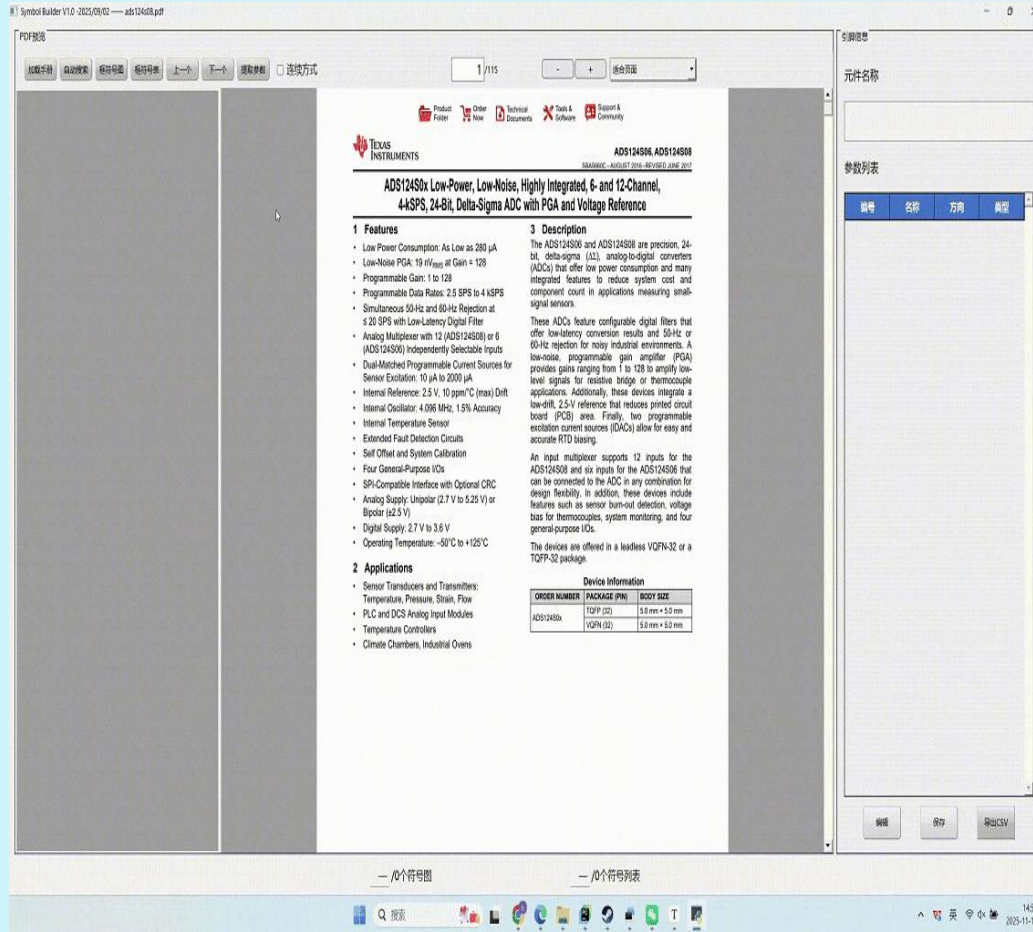
Data Properties(CoreDevice 实例)

- └-- ADS124S06_Chip01 (CoreDevice_ADS124S06)
 - └-- 具有封装类型: Package_TQFP-PBS_32Pin
 - └-- 关联器件: OrderablePart_ADS124S06IPBSG4, OrderablePart_ADS124S06IPBSR
 - └-- 包含管脚: Pin_AIN0, Pin_AVSS-SW, Pin_CS, Pin_SCLK
- └-- **ADS124S08_Chip01 (CoreDevice_ADS124S08)**
 - └-- 具有封装类型: **Package_VQFN-RHB_32Pin**
 - └-- 关联器件: **OrderablePart_ADS124S08IRHBRG4, OrderablePart_ADS124S08IRHBT**
 - └-- 包含管脚: **Pin_AIN0, Pin_AVSS-SW, Pin_CS, Pin_SCLK, Pin_REFOUT.....**

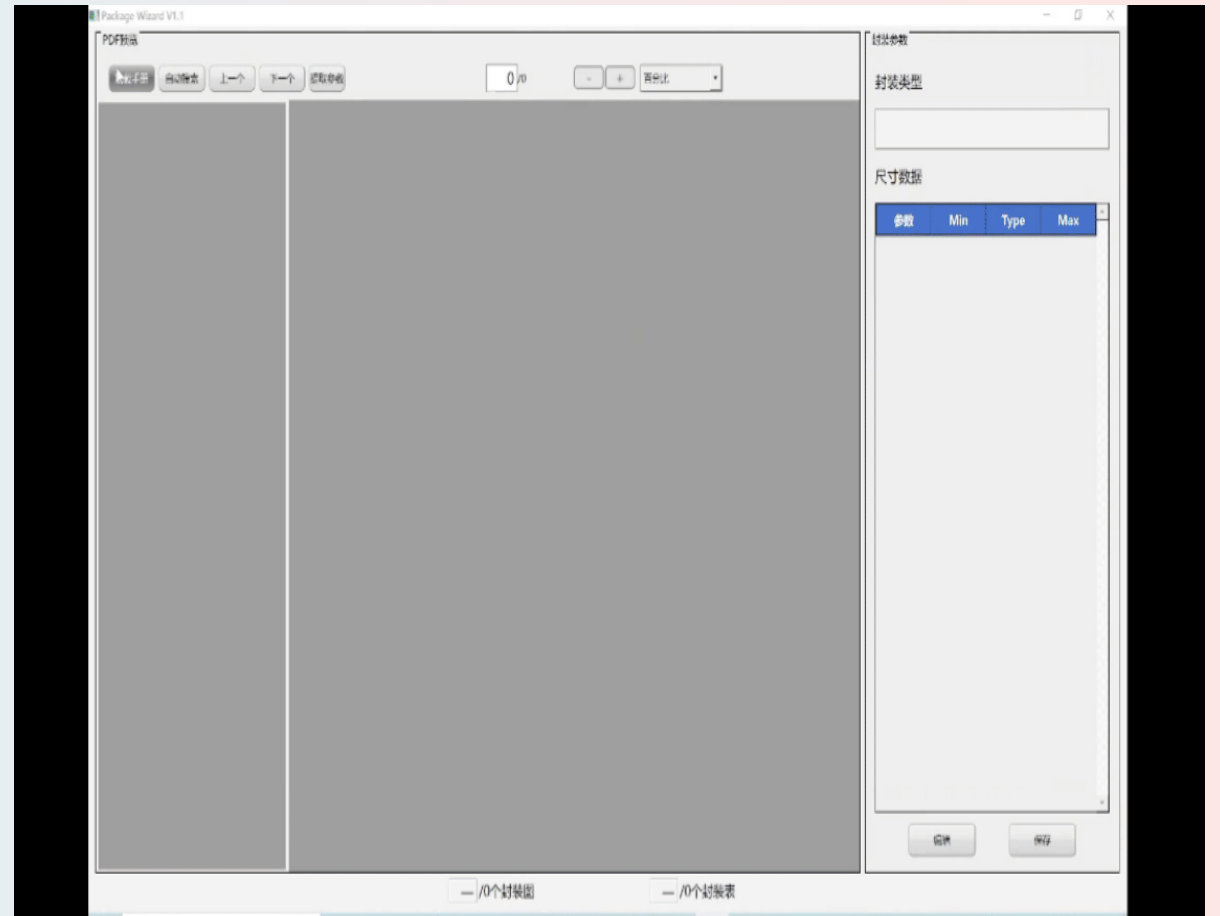
What roles should be assigned to the AI agent in PDF datasheets?



How are we connecting our tools to complement KiCad?



Symbol+Kicad



Package+Kicad



How can AI Agents, powered by Large Language Models(LLMs), enhance their accuracy?



The sobering reality where the magic of LLMs runs out?

Our Symbol Agent empowers you to work within:

- 1) High Density QFN/QFP
- 2) Big Array of BGA

Symbol Builder V1.0 - 2025/09/02 — dac5682z.pdf

PDF预览

加载手册 自动搜索 框符号图 框符号表 上一个 下一个 提取参数 连续方式

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Product Folder Sample & Buy Technical Documents Tools & Software Support & Community Reference Design

TEXAS INSTRUMENTS

DAC5682Z

SLLS883F - AUGUST 2007 - REVISED JANUARY 2015

DAC5682Z 16-Bit, 1.0 GSPS 2x-4x Interpolating Dual-Channel Digital-to-Analog Converter (DAC)

1 Features

- 16-Bit Digital-to-Analog Converter (DAC)
- 1.0 GSPS Update Rate
- 16-Bit Wideband Input LVDS Data Bus
 - 8 Sample Input FIFO
 - Interleaved IQ Data for Dual-DAC Mode
- High Performance
 - 73-dBc ACLR WCDMA TM1 at 180 MHz
 - 2x-32x Clock Multiplying PLL/VCO
- 2x or 4x Interpolation Filters
 - Stopband Transition 0.4 to 0.6 Fdata
 - Filters Configurable in Either Low-Pass or High-Pass Mode
 - Allows Selection of Higher Order Image
- Fs/4 Coarse Mixer
- On-Chip 1.2-V Reference
- Differential Scalable Output: 2 to 20 mA
- Package: 64-Pin 9-mm × 9-mm QFN

2 Applications

- Cellular Base Stations
- Broadband Wireless Access (BWA)
- WiMAX 802.16
- Fixed Wireless Backhaul
- Cable Modem Termination System (CMTS)

3 Description

The DAC5682Z is a dual-channel 16-bit 1.0 GSPS DAC with wideband LVDS data input, integrated 2x/4x interpolation filters, onboard clock multiplier, and internal voltage reference. The DAC5682Z offers superior linearity, noise, crosstalk, and PLL phase noise performance.

The DAC5682Z integrates a wideband LVDS port with on-chip termination. Full-rate input data can be transferred to a single DAC channel, or half-rate and 1/4-rate input data can be interpolated by onboard 2x or 4x FIR filters. Each interpolation FIR is configurable in either low-pass or high-pass mode, allowing selection of a higher order output spectral image. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (MM)
DAC5682Z	QFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

3-Carrier WCDMA TM1 With a Gap

Power - dBm

f - Frequency - MHz

Carrier Power: -45.20 dBm
ACLR @ 180 MHz: 71.18 dB
ACLR @ 180 MHz: 72.26 dB
F_{data} = 491.52 MHz
F_{clk} = 195.76 MHz
2x Interpolation
PLL Off

编辑 保存 导出CSV

元件名称

参数列表

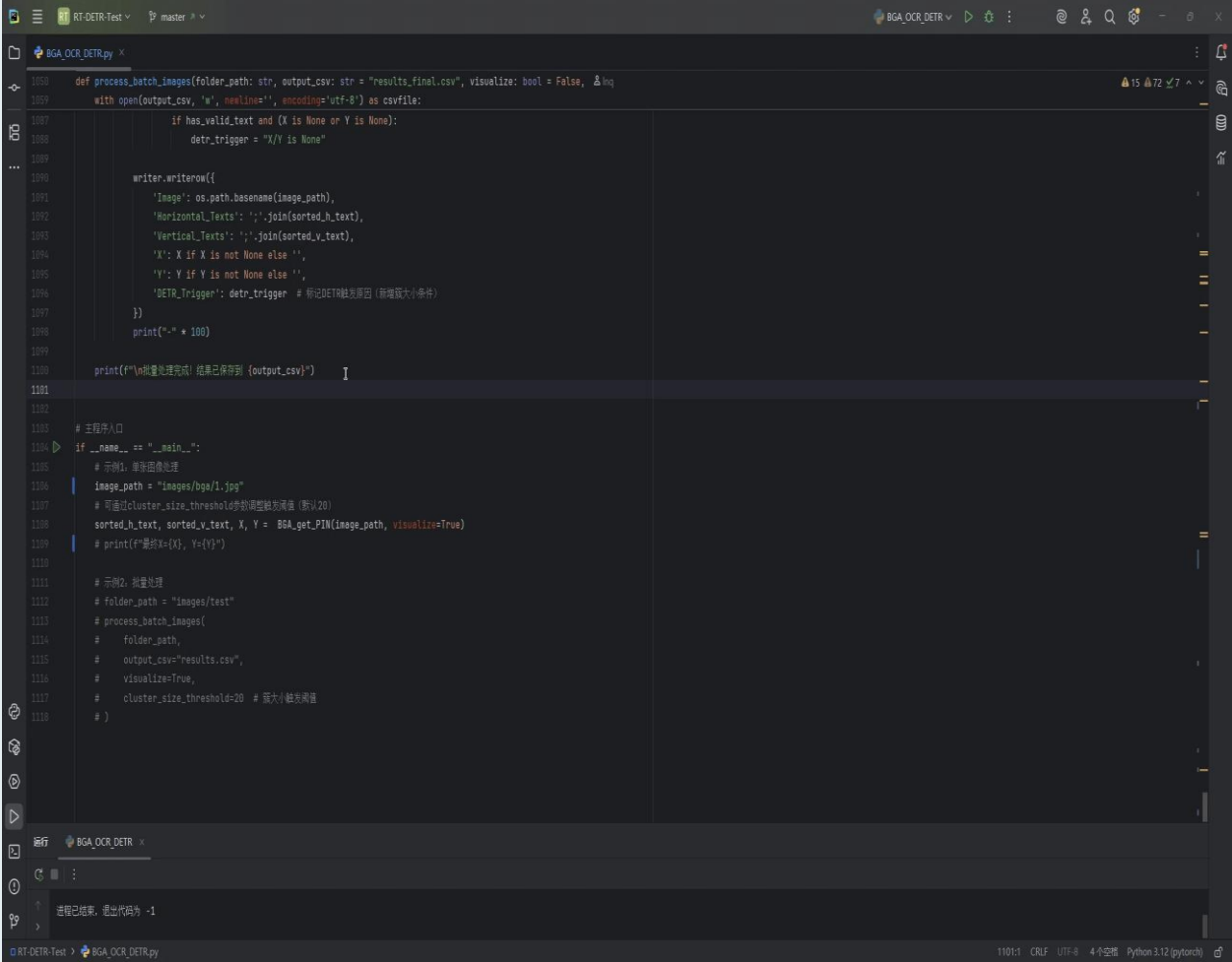
编号	名称	方向	类型
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— /0个符号图 — /0个符号列表

The sobering reality where the magic of LLMs runs out?

Our Package Agent
epowers, you to work within:

- 1) The position of Pin 1;
- 2) Calculating Row and Column Counts in a BGA
- 3) Handling of Missing Solder Balls in a BGA
- 4) All the pins caculation in different packages



```
def process_batch_images(folder_path: str, output_csv: str = "results_final.csv", visualize: bool = False,
                          with_open(output_csv, "w", newline="", encoding="utf-8") as csvfile:
    if has_valid_text and (X is None or Y is None):
        detr_trigger = "X/Y is None"

    writer.writerow([
        'Image': os.path.basename(image_path),
        'Horizontal_Texts': ': '.join(sorted_h_text),
        'Vertical_Texts': ': '.join(sorted_v_text),
        'X': X if X is not None else '',
        'Y': Y if Y is not None else '',
        'DETR_Trigger': detr_trigger # 标记DETR触发原因 (新增大小条件)
    ])
    print("-" * 100)

print(f"\n批量处理完成! 结果已保存到 {output_csv}")

# 主程序入口
if __name__ == "__main__":
    # 示例1: 单张图像处理
    image_path = "images/bga/1.jpg"
    # 可通过cluster_size_threshold的参数调整触发阈值 (默认20)
    sorted_h_text, sorted_v_text, X, Y = BGA_get_PIN(image_path, visualize=True)
    # print(f"检测到X={X}, Y={Y}")

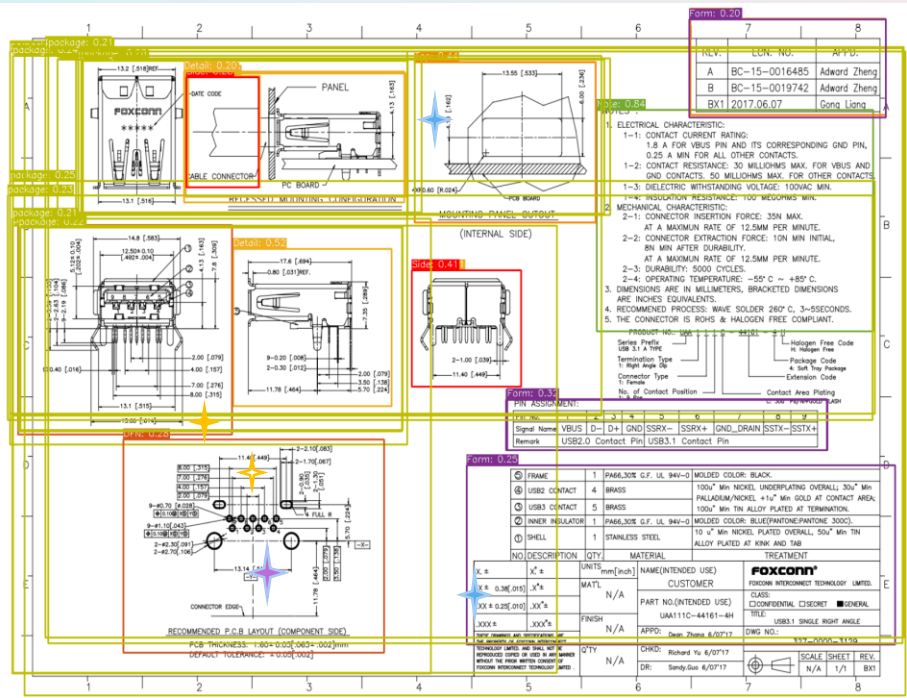
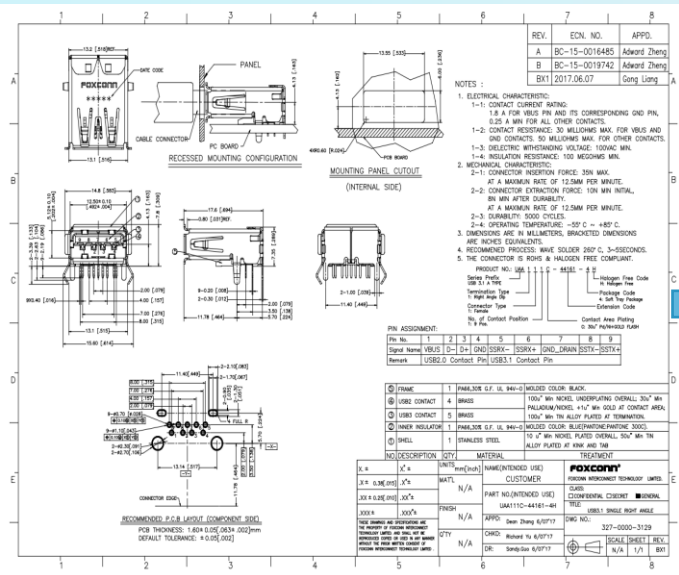
    # 示例2: 批量处理
    # folder_path = "images/test"
    # process_batch_images(
    #     folder_path,
    #     output_csv="results.csv",
    #     visualize=True,
    #     cluster_size_threshold=20 # 簇大小触发阈值
    # )
```



01

Anything Else ?

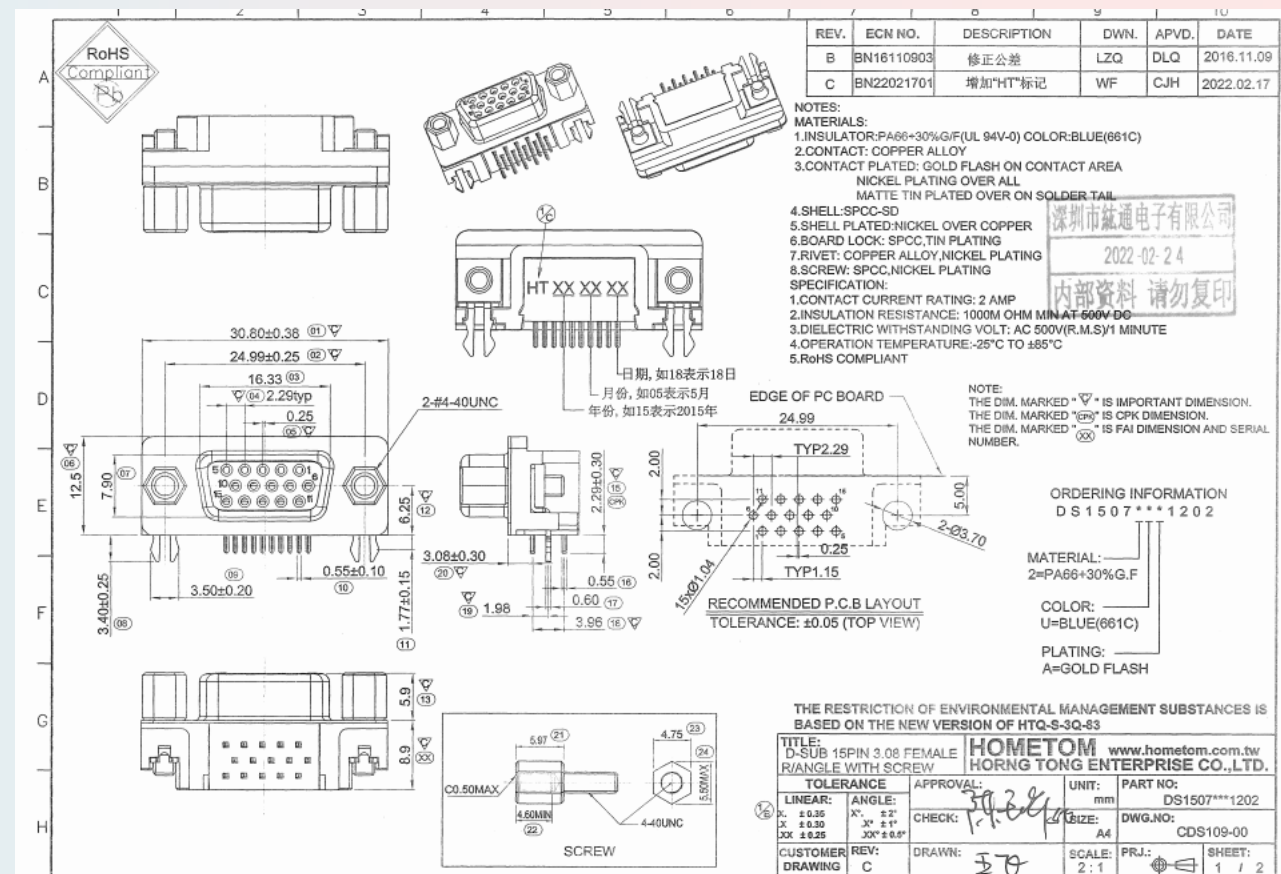
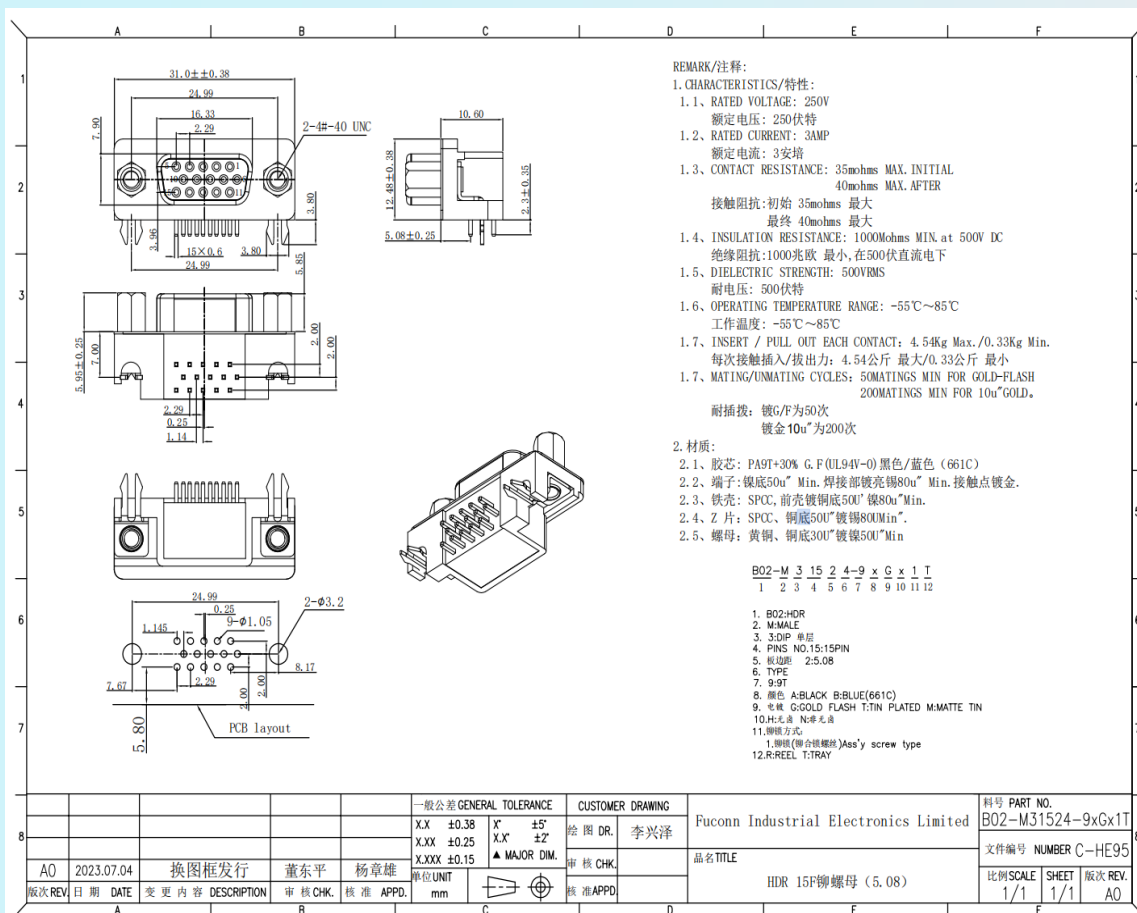
Non-standard Component Analysis



Parameter	USB
Signal Pin Count	9
Positioning Pin Count	4
Body Length (A)	17.6
Body Width (B)	13.2
Body Height (H)	7.35
Signal Pin Pitch	1.1
Signal Pin Diameter	0.7
Positioning Pin Pitch 1 (Round)	2.7
Positioning Pin Diameter 1 (Round)	2.3
Positioning Pin Pitch 2 (Ellipse, 2 pcs Long Axis)	2.1X1.3
Positioning Pin Diameter 2 (Ellipse, 2 pcs Long Axis)	1.7X0.9
Signal Pin pitch1	2
Signal Pin pitch2	4
Signal Pin pitch3	7
Signal Pin pitch4	8
Positioning Pin pitch1	11.4
Positioning Pin pitch2	13.14

Layout Analysis + Graphic Similarity Analysis (Locking Key Feature Views)

Component Similarity Analysis



- 1) Analyze the component type in the image and output the physical dimension parameters of its package;
- 2) Extract the text content in the image, Comprehend the table content;
- 3) Compare the image content, text content, and table content of the two images, identify similarities and differences, and provide a summary conclusion.

Component Part Number Usage by Role



Role	Focus	Part Number Used	Core Question
Design Engineer	Function, performance, pinout of the component	Full Orderable Part Number	"Can I use it in my circuit?"
Procurement / Supply Chain	Exact specifications, procurement availability, price, lead time	Full Orderable Part Number	"Can we buy the correct one?"
PCB / Manufacturing Engineer	Physical dimensions, footprint, assembly process	Package portion within the Orderable Part Number	"Can we solder it to the board?"





EDA's adventure is still a long, tough road ahead!



吴绿

