KiCad,连接梦想和现实的纽带

KICAD,THE BRIDGE CONNECTING DREAMS AND REALITY

半糖 HalfSweet

Try to create some value

https://github.com/HalfSweet/

halfsweet@halfsweet.cn

https://space.bilibili.com/113604828

@HalfSweet

我的硬件经历

My Hardware Journey

样板　2020-06-27 17:05:52　订单编号：Y1

USB_typec (2)

双面板　5片　1.6　哑黑色　有铅喷锡

正常3天

￥5.00　包邮

在线支付价

返单　查看生产稿

改为需SMT　评价晒单　下激光钢网

订单详情

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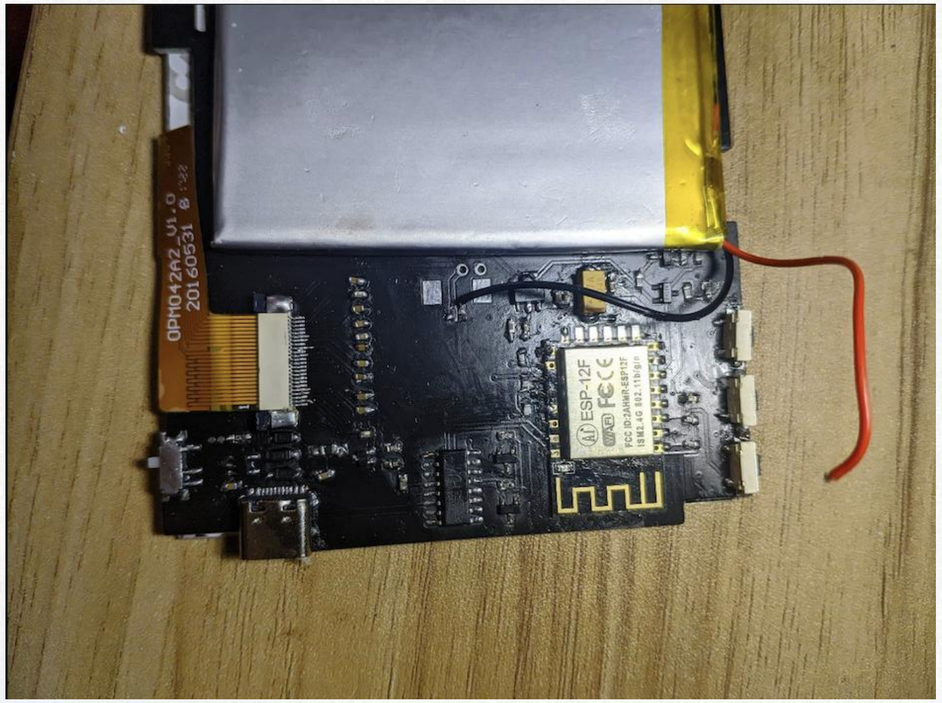

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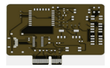

远程开机

双面板　5片　1.6　哑黑色　有铅喷锡

正常3天

包邮

￥5.00

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返单　查看生产稿

改为需SMT　评价晒单　下激光钢网

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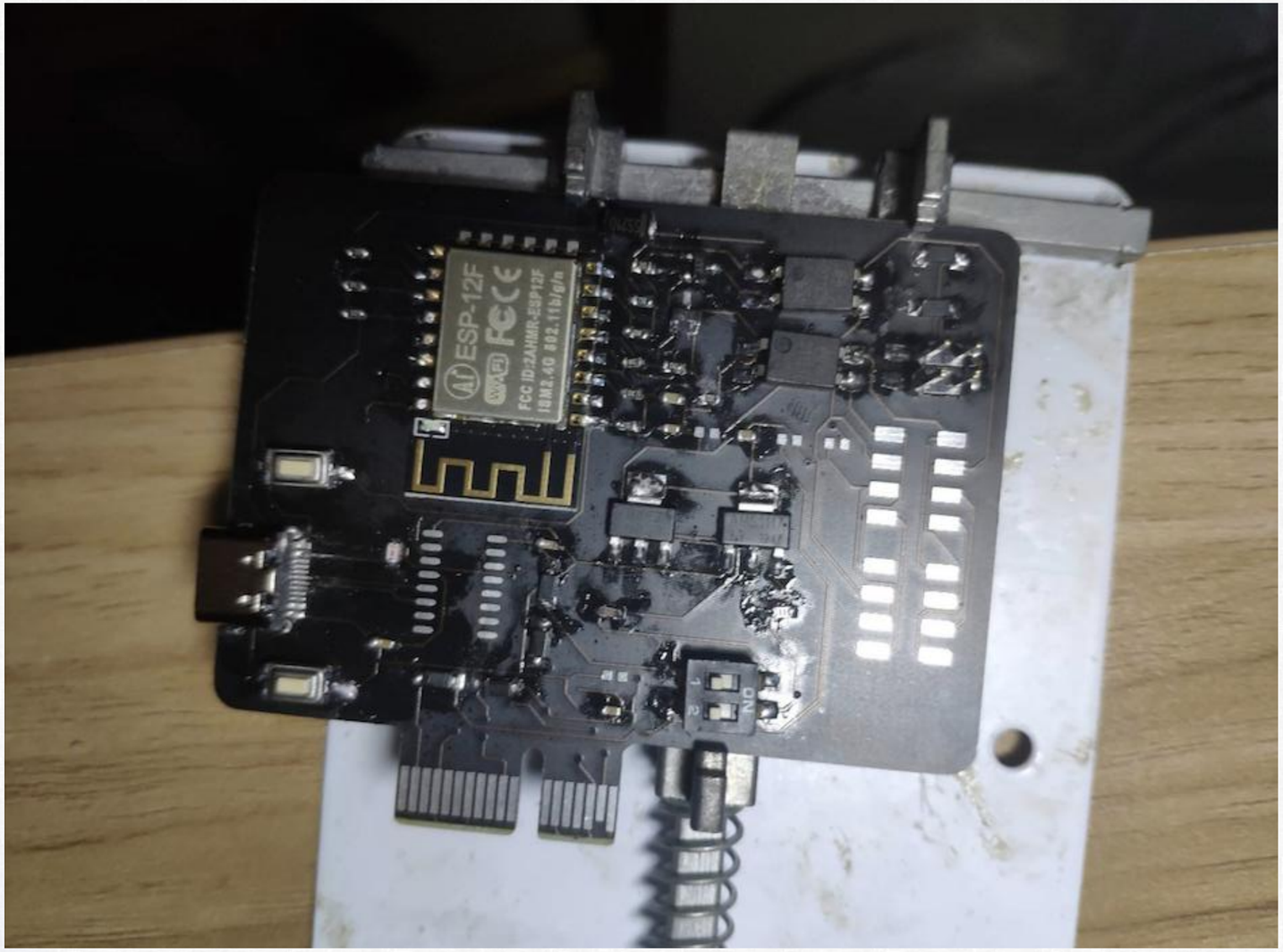

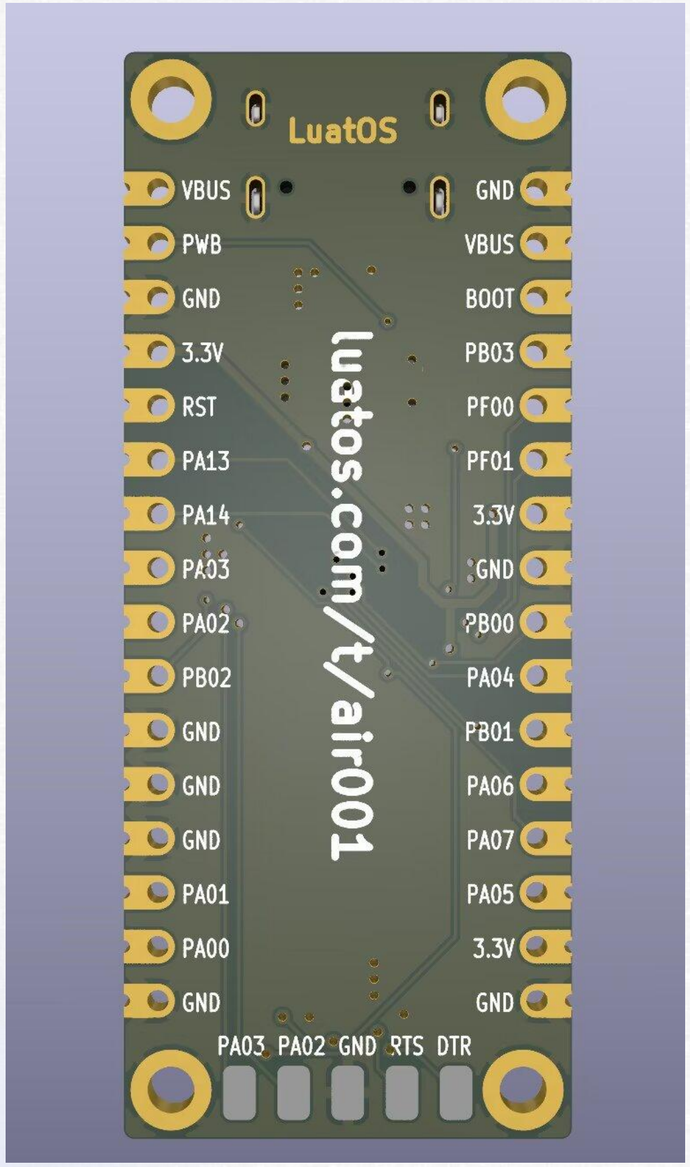
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GND
VBUS
BOOT
PB03
PF00
PF01
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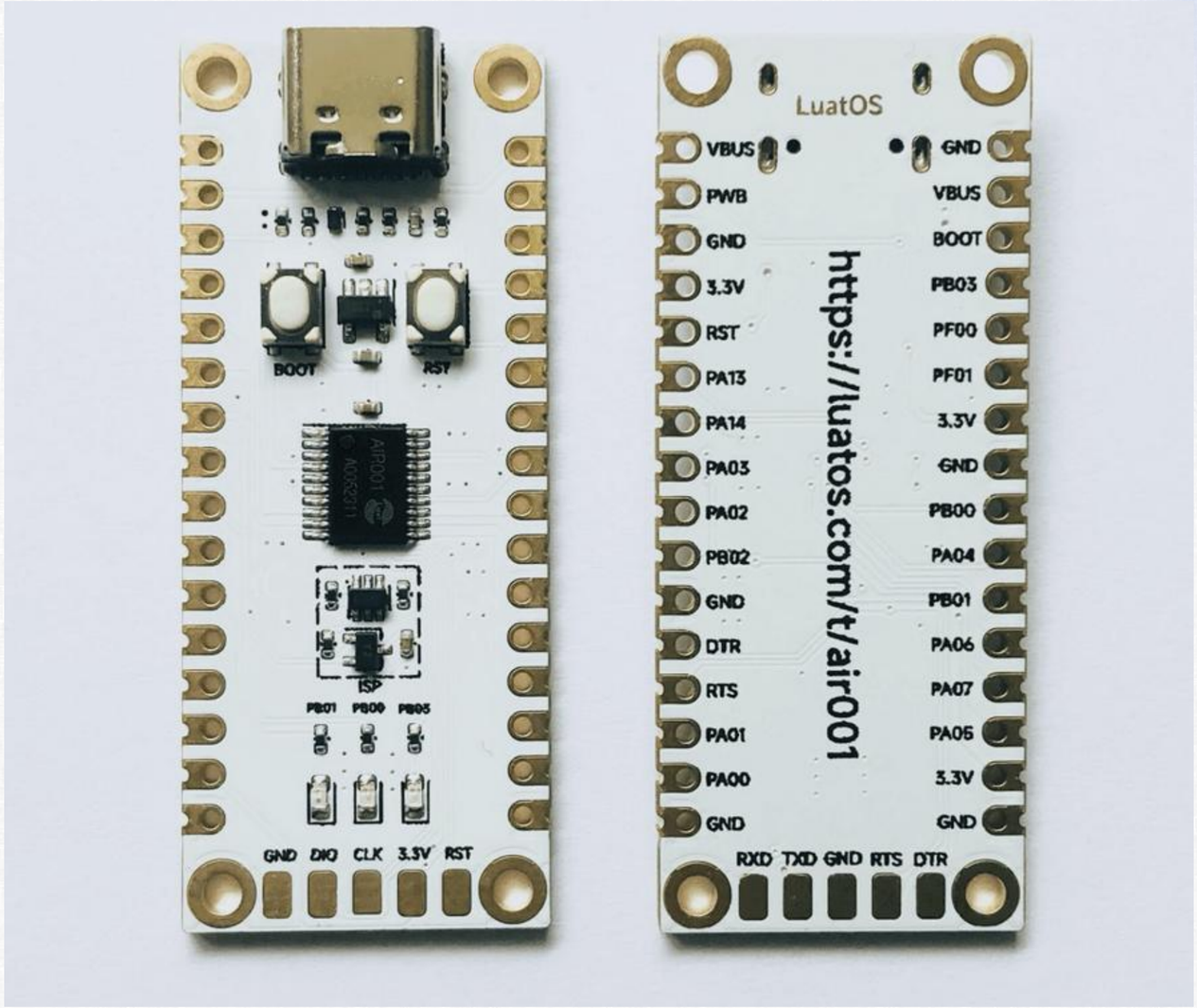
luatos.com/t/air001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PF01
3.3V
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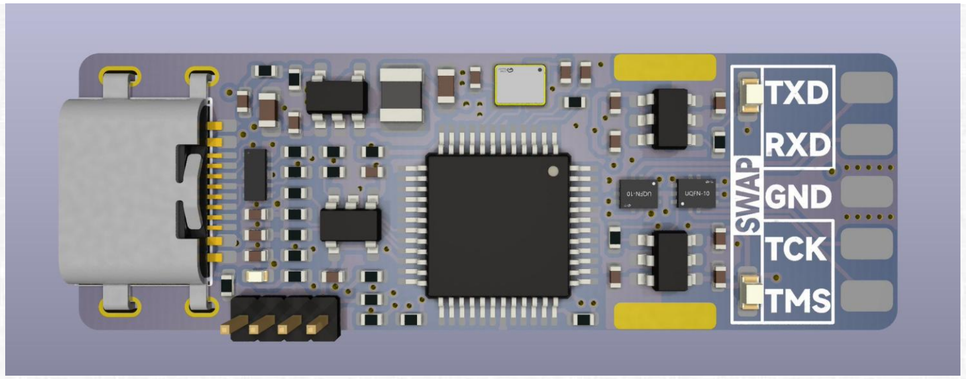
https://luatos.com/t/air001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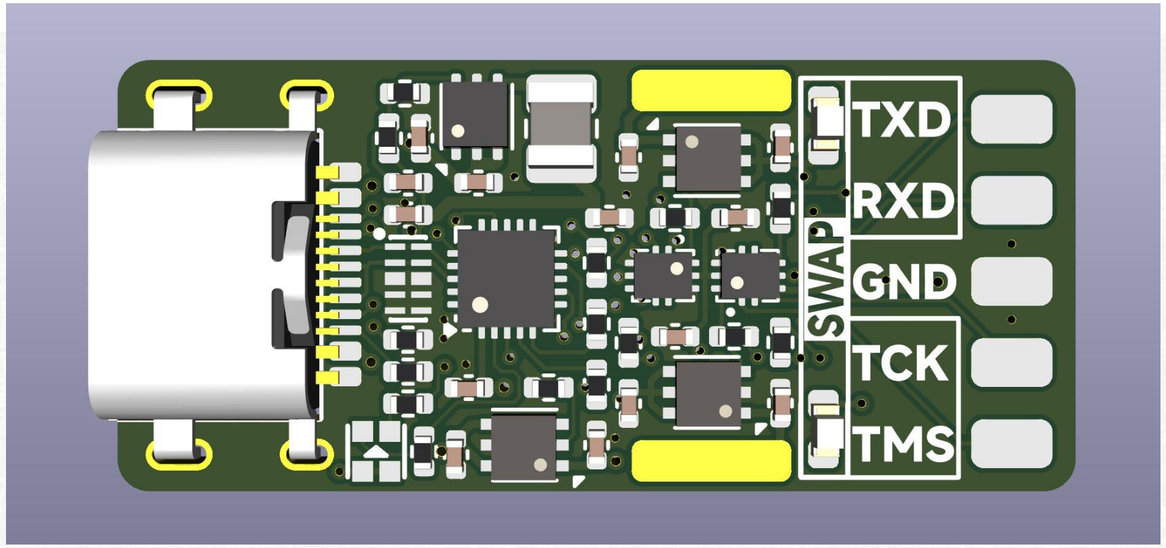
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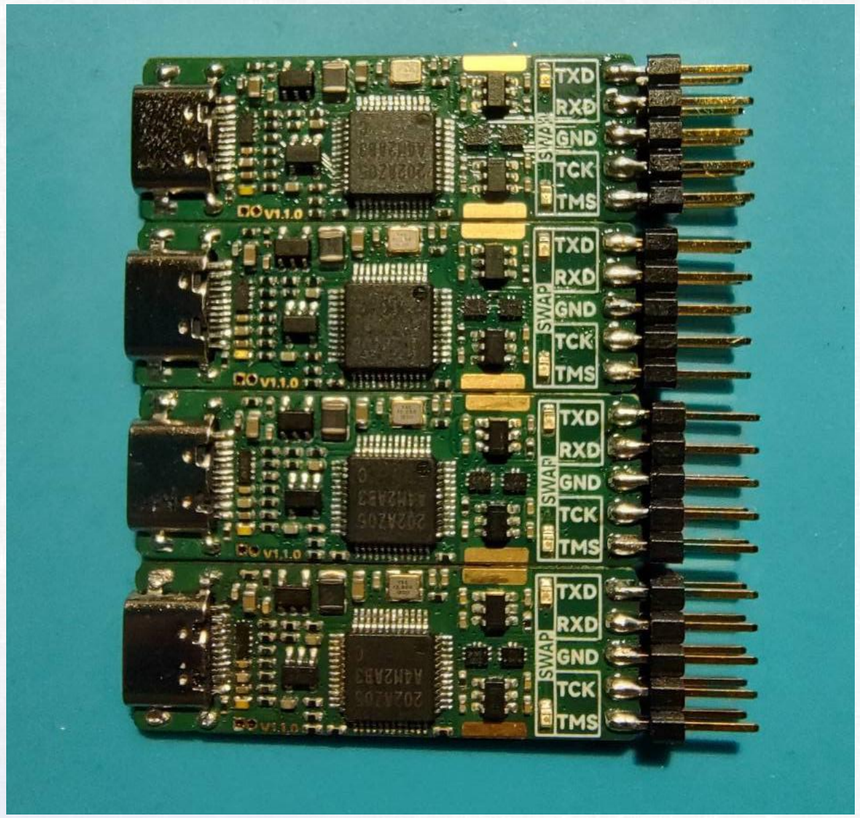
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GND
TCK
TMS
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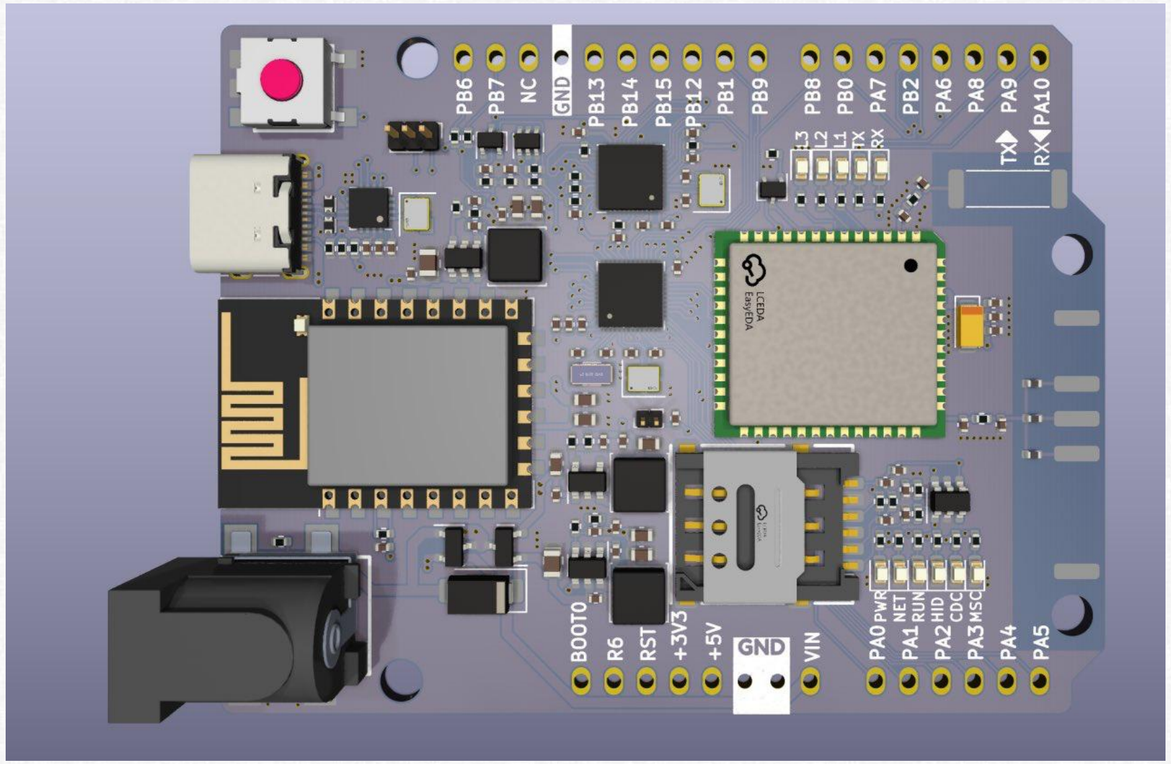
Jlink-OB-RA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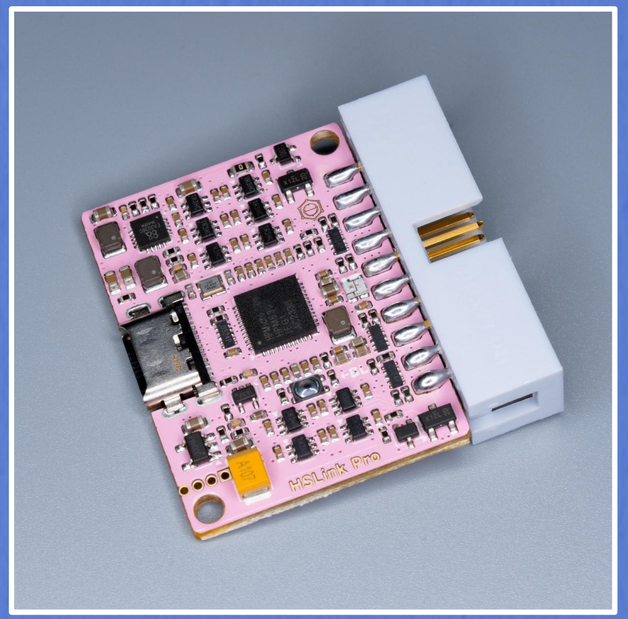
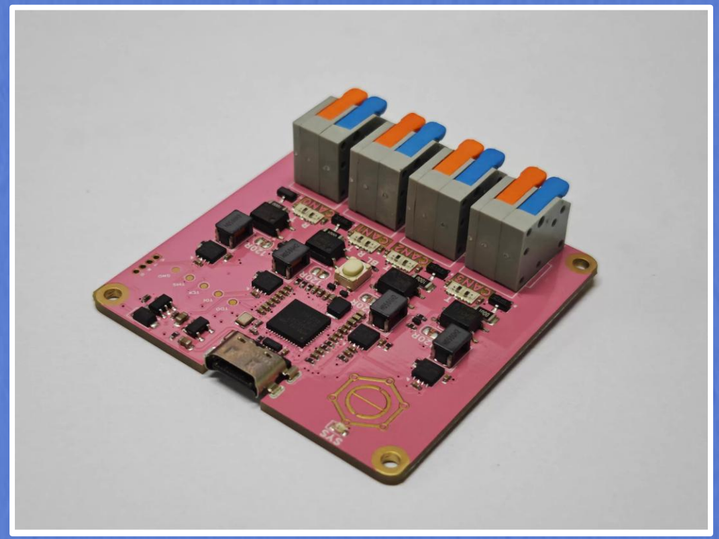
PB9
PB8
PB0
PA7
PB2
PA6
PA8
PA9
PA10
L3
L2
L1
TX
RX
TX
RX
LCEDA
EasyEDA
BOOT0
R6
RST
+3V3
+5V
GND
VIN
PA0 PWR
PA1 NET
PA2 HID
PA3 MSC
PA4
PA5
RUN
CDC

HSLink Pro

- 80M SWD/JTAG
- 1.8-5V Level support and power output capability, 1A max
- CDC DTR/RTS support
- https://cherrydap.cherry-embedded.org/projects/HSLink%20Pro

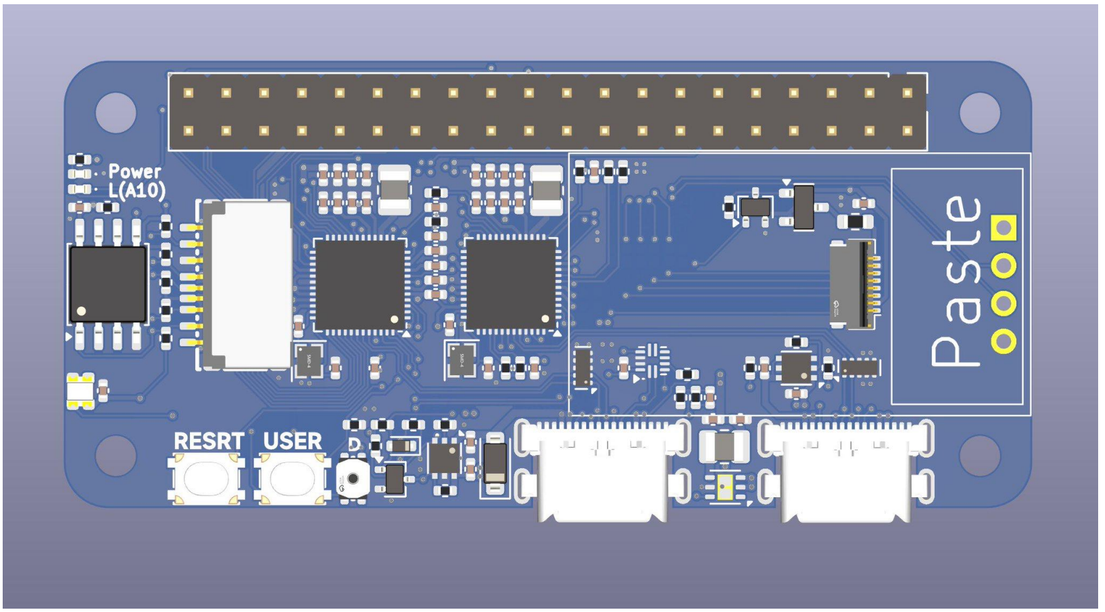


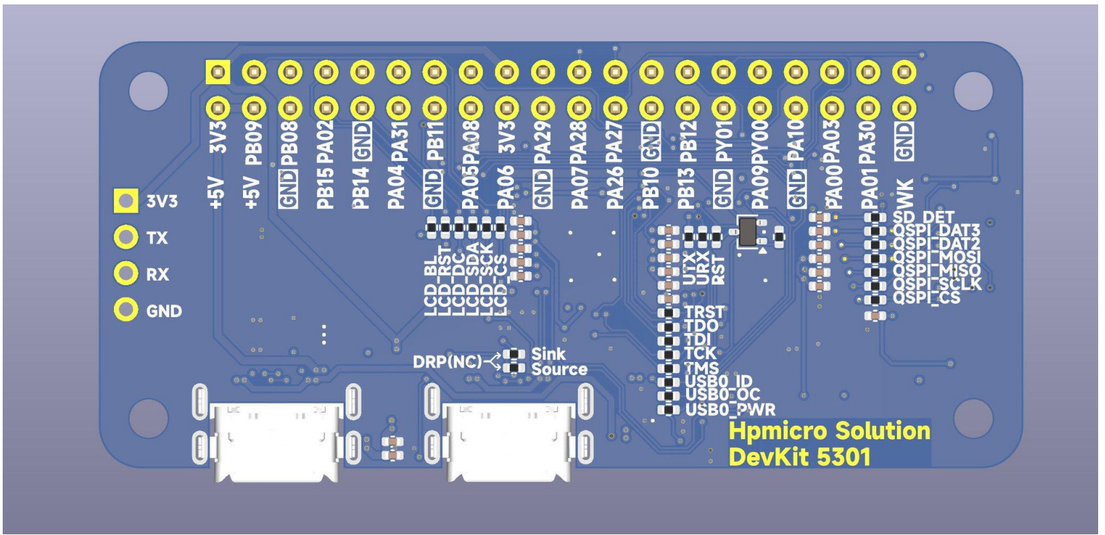


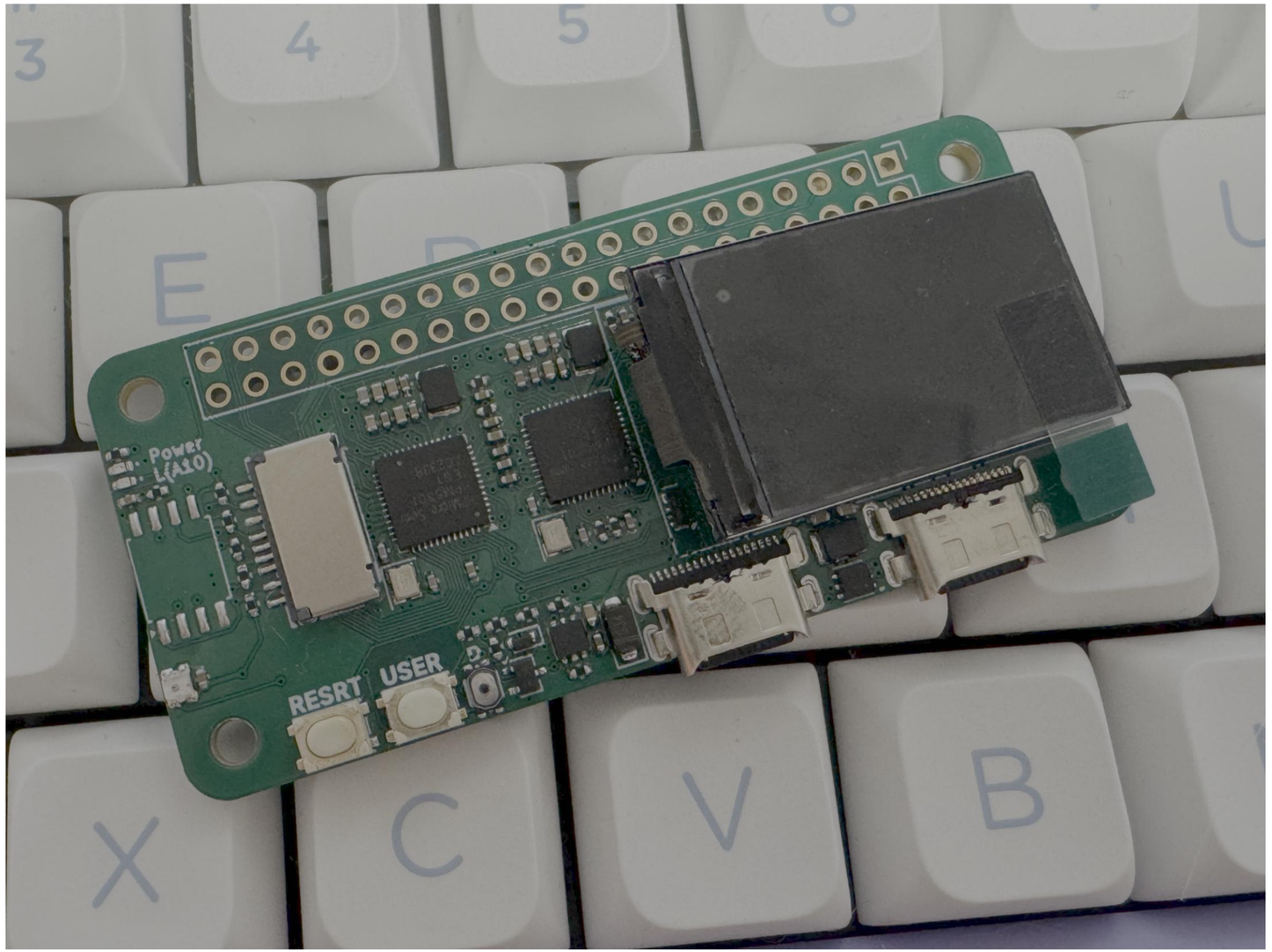
HSCanT

- 4 channel 8M CAN FD
- Slcan/GS USB support, dynamic switch
- Ecubus Pro
- https://hscant.cherry-embedded.org/

HSDevKit5301





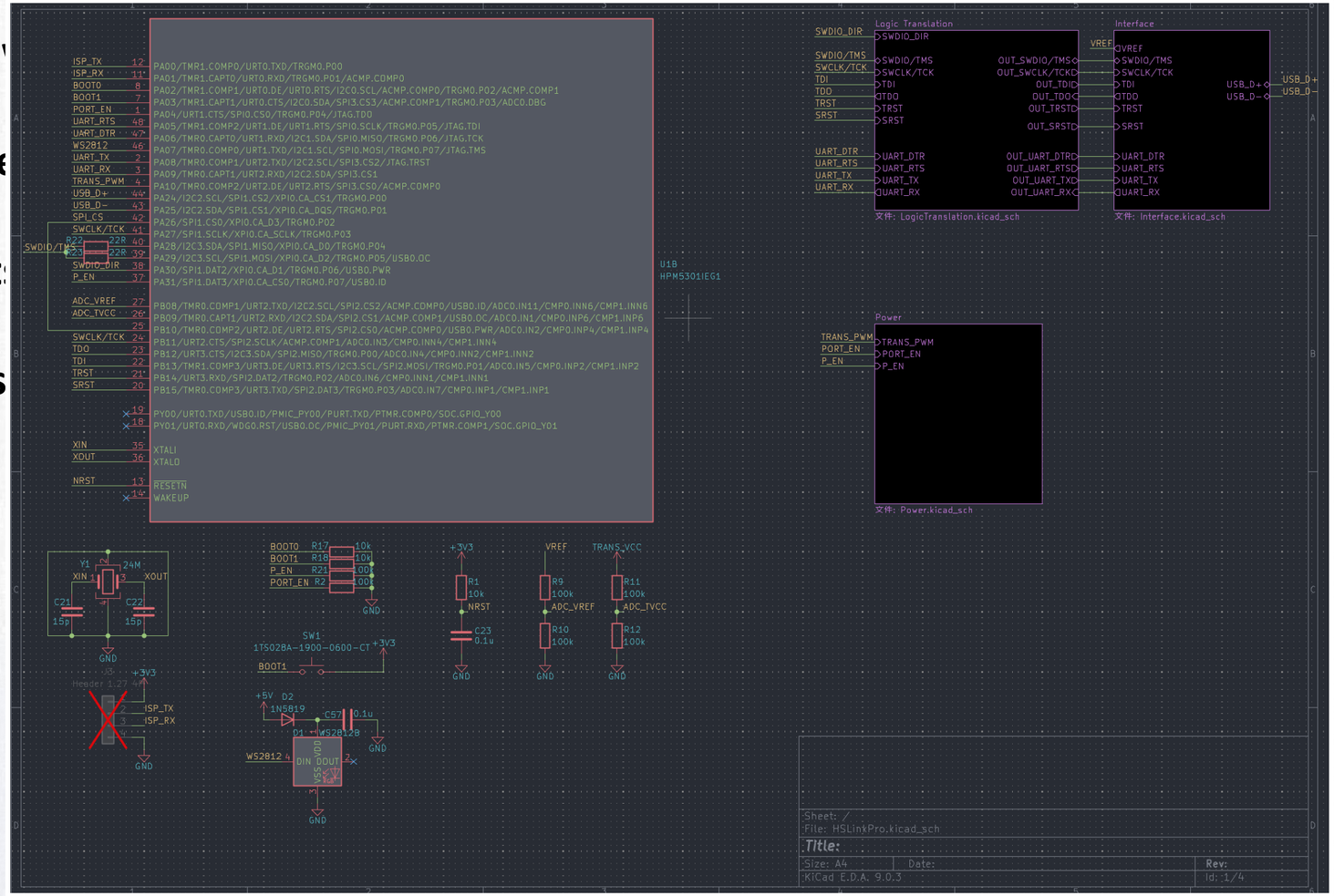


Why KiCad?

- Native cross-platform support
- Powerful performance that still runs smoothly on lower end devices
- Plain text document format, Git friendly, easy to integrate
- Open Source! A community of freedom, where your copyright always belongs to you
- I can contribute to the community
- A rich API and plugin system that provides great flexibility and fosters a highly engaged community
- CI/CD-friendly, with kicad-cli and open file formats that facilitate automation.

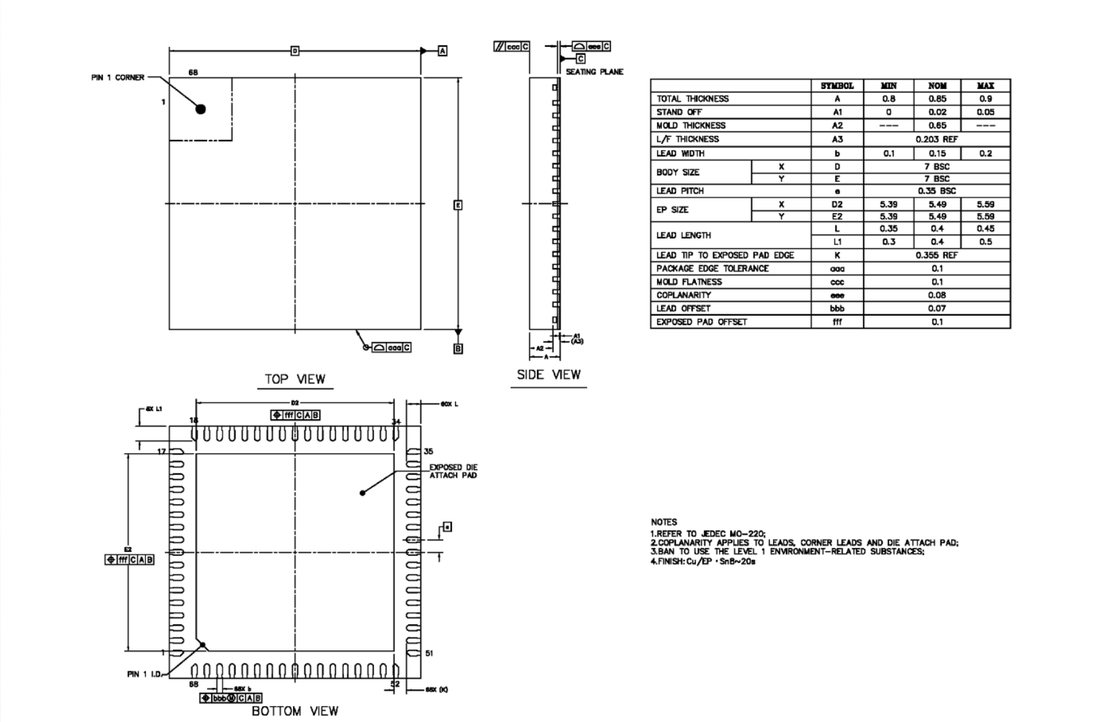
Disadvantages of KiCAD?

- **The library is still missing many non-standard components; even though the library maintainers**
- **Content gene requirement**
- **MCUs have s**



Describe using structured data

- **Footprint**



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.1	0.15	0.2
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	5.39	5.49	5.59
	Y	E2	5.39	5.49	5.59
LEAD LENGTH		L	0.35	0.4	0.45
		L1	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.355 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP：SnB~20u

```yaml
packages:
  - name: QFN-68-1EP_7x7mm_P0.35mm_EP5.49x5.49mm
    size_source: "https://downloads.sifli.com/user%20manual/DS52
    device_type: QFN
    ipc_class: qfn_pull_back
    num_pins_x: 17
    num_pins_y: 17      You, 前天 • feat: 添加封装 …
    pitch: 0.35
    body_size_x:
      nominal: 7.0
      tolerance: 0.1
    body_size_y:
      nominal: 7.0
      tolerance: 0.1
    overall_height:
      minimum: 0.85
      nominal: 0.9
      maximum: 0.95
    lead_width:
      minimum: 0.10
      nominal: 0.15
      maximum: 0.20
    lead_len:
      minimum: 0.35
      nominal: 0.40
      maximum: 0.45
    EP_size_x:
      minimum: 5.39
      nominal: 5.49
      maximum: 5.59
    EP_size_y:
      minimum: 5.39
      nominal: 5.49
      maximum: 5.59
    EP_num_paste_pads: [3, 3]
    thermal_vias:
      count: [4, 4]
      drill: 0.2
      EP_paste_coverage: 0.6
      paste_via_clearance: 0.1
```

Describe using structured data

- **Structured Data Built Around the Chip**

```yaml
pads:
  PA00: &PA00
    type: bidirectional
    pinmux:
      - {function: GPIO_A0, select: 0}
      - {function: LCDC1_SPI_RSTB, select: 1}
      - {function: I2C, select: 4}
      - {function: UART, select: 4}
      - {function: TIM, select: 5}
      - {function: LCDC1_8080_RSTB, select: 7}
  PA01: &PA01
    type: bidirectional
    pinmux:
      - {function: GPIO_A1, select: 0}
      - {function: I2C, select: 4}
      - {function: UART, select: 4}
      - {function: TIM, select: 5}
  PA02: &PA02
    type: bidirectional
    pinmux:
      - {function: GPIO_A2, select: 0}
      - {function: LCDC1_SPI_TE, select: 1}
      - {function: I2S1_MCLK, select: 3}
      - {function: I2C, select: 4}
      - {function: UART, select: 4}
      - {function: TIM, select: 5}
      - {function: LCDC1_JDI_B2, select: 6}
      - {function: LCDC1_8080_TE, select: 7}
```

```yaml
variants:
  - part_number: SF32LB520U36
    description: "8Mb NOR Flash"
    package: QFN-68-1EP_7x7mm_P0.35mm_EP5.49x5.49mm
    pins: &SF32LB52x_QFN68_PINS
      - {number: 1, pad: *PA32}
      - {number: 2, pad: *PA31}
      - {number: 3, pad: *PA30}
      - {number: 4, pad: *PA29}
      - {number: 5, pad: *PA28}
      - {number: 6, pad: *PA27}
      - {number: 7, pad: *PA26}
      - {number: 8, pad: *PA25}
      - {number: 9, pad: *PA24}
      - {number: 10, pad: *PA23}
      - {number: 11, pad: *PA22}
      - {number: 12, pad: *VDD_RTC}
      - {number: 13, pad: *VDD_RET}
      - {number: 14, pad: *VDD33_VOUT2}
      - {number: 15, pad: *VDD_VOUT2}
      - {number: 16, pad: *VDD_VOUT1}
      - {number: 17, pad: *BUCK_FB}
      - {number: 18, pad: *BUCK_LX}
      - {number: 19, pad: *VSYS}
      - {number: 20, pad: *VBAT}
      - {number: 21, pad: *VBUS}
      - {number: 22, pad: *VDD33_VOUT1}
      - {number: 23, pad: *VDD18_VOUT}
      - {number: 24, pad: *VCC}
      - {number: 25, pad: *PA20}
```

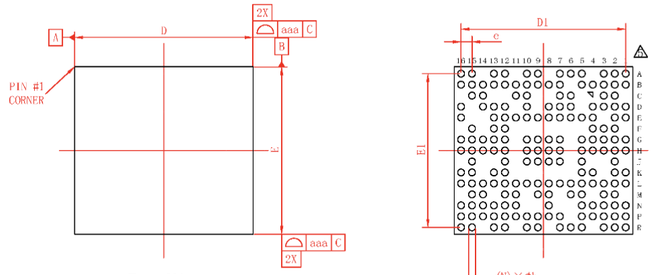
```yaml
  - part_number: SF32LB523UB6
    description: "32Mb OPI-pSRAM"
    package: QFN-68-1EP_7x7mm_P0.35mm_EP5.49x5.49mm
    pins: *SF32LB52x_QFN68_PINS
  - part_number: SF32LB525UC6
    description: "64Mb OPI-pSRAM"
    package: QFN-68-1EP_7x7mm_P0.35mm_EP5.49x5.49mm
    pins: *SF32LB52x_QFN68_PINS
  - part_number: SF32LB527UD6
    description: "128Mb OPI-pSRAM"
    package: QFN-68-1EP_7x7mm_P0.35mm_EP5.49x5.49mm
    pins: *SF32LB52x_QFN68_PINS
```

Describe using structured data

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	PVDD	VDD_RTC		PA55	PA56	PA65		PA73	PBR0		XTAL48M_XI	XTAL48M_XO		PB35	VSS	A
B	BUCK_LX	BUCK_FB	LDO1_VOUT	VDD_RET	VSS		PA64	PA69	PA71	PBR1	PBR3	AVSS	AVSS_RF4	PB36	PB31	PB30	B
C		LDO2_VOUT	PA52			PA60	PA62			PA78	PA75			PB34	PB29		C
D	BOOT_MODE	PA53	PA54	PA58		PA57	PA63	PA67		PA76		PBR2	PB32	PB33		AVSS_RF1	D
E	PA51	PA50		PVSS	VSS	PA61	PA66	PA68	PA70	PA72	PA74	PA77	VSS			BRF_ANT	E
F		PA49	PA48	PA59								VSS	MIC_BIAS		AVSS_RF2		F
G	PA46	PA45	PA44	PA47	PA42		VSS	VSS	VSS	PB5		VSS	ADCN	ADCP	AVSS_RF3	AVDD_BRF	G
H	VDDIOSA	VDDIOSB	PA43	PA40	PA39		VSS	VSS	VSS	PB4		VSS	AUD_VREF	AVSS	AVDD33_ANA	AVDD33_AUD	H
J		PA41			PA37		PA10	VSS	VSS	VDDIOB		PB9			AVSS		J
K	PA35	PA38		PA36	PA31							PB11	PB22		DACP	DACN	K
L	PA33	PA34	PA32	PA29	PA16	VDDIOA	PA7	VDDIOA2	PA3	PB0	PB1	VSS	PB23	PB24	GPADC_VREFP	AVSS	L
M		PA30	PA28		PA14	PA11		PA6	PA2		PB3	PB17		PB26	PB28		M
N	PA26	PA27	PA25	PA24	PA13			PA4			PB7	PB16	PB10	PB14	PB25	PB27	N
P	PA20	PA23	PA19	PA18	PA17		PA9	PA5	PA1	PB2	PB6	PB15	PB8	PB18	PB19	PB20	P
R	VSS	PA21	PA22		PA15	PA12	PA8		PA0	VDDIOSC		PB13	PB12		PB21	VSS	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

图 5-1: SF32LB565/SF32LB566/SF32LB567（BGA175）管脚布局（俯视图）

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
A1	0.130	0.180	0.230	0.005	0.007	0.009
A2	0.710	0.760	0.810	0.028	0.030	0.032
c	0.180	0.220	0.260	0.007	0.009	0.010
D	6.400	6.500	6.600	0.252	0.256	0.260
E	6.000	6.100	6.200	0.236	0.240	0.244
D1	----	6.000	----	----	0.236	----
E1	----	5.600	----	----	0.220	----
e	----	0.400	----	----	0.016	----
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.250			0.010		
N	175			175		
MD/ME	16/15			16/15		



TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.230mm; [球形防焊开口: 0.230mm;]

△PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
[主要基准C和底面是锡球;]

△DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]

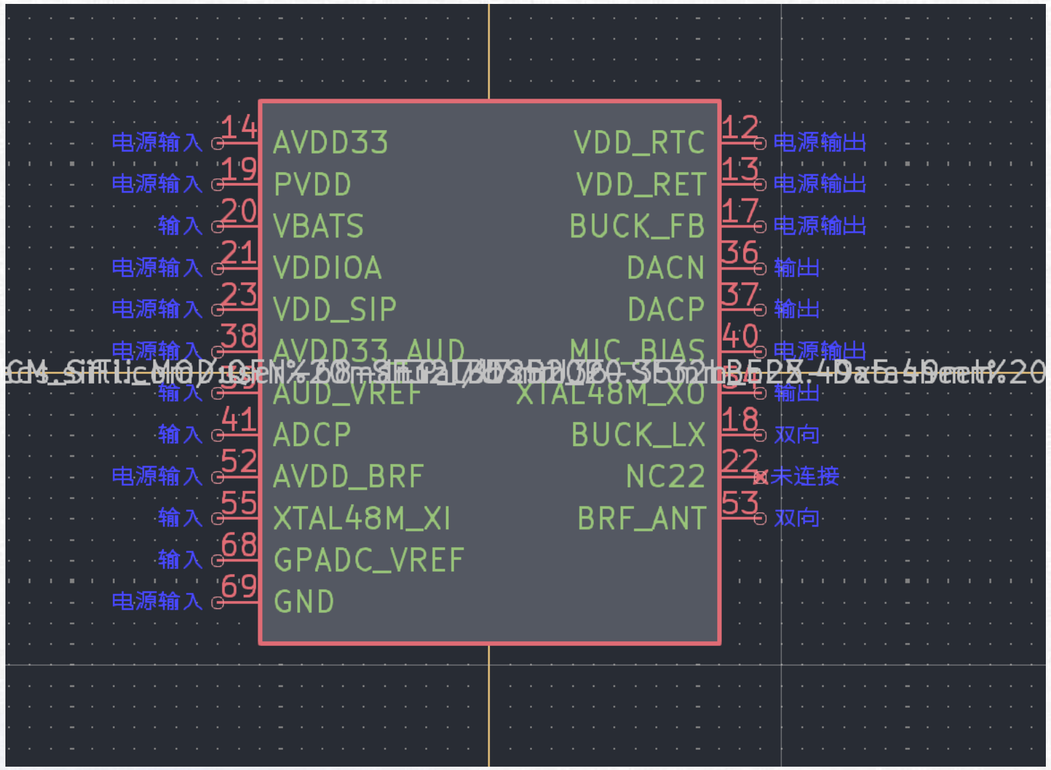
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]

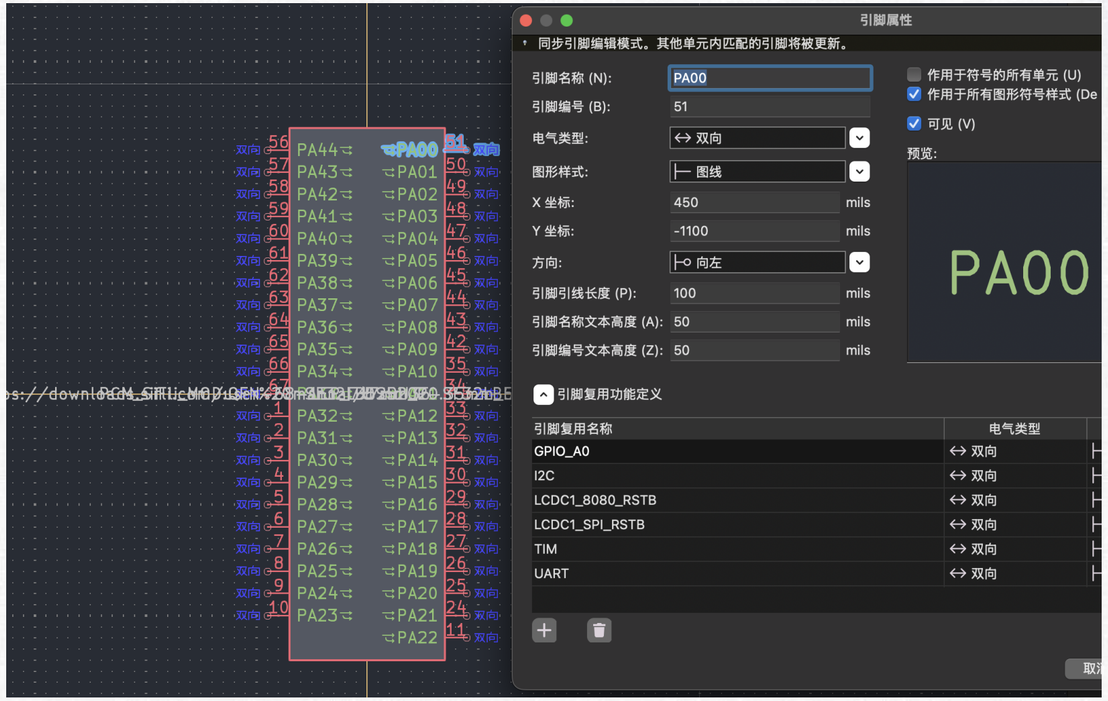
△THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
[PIN 1 标识仅供参考;]

6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
[禁止使用一级环境管理物质;]

图 5-4: BGA175 封装尺寸

Describe using structured data

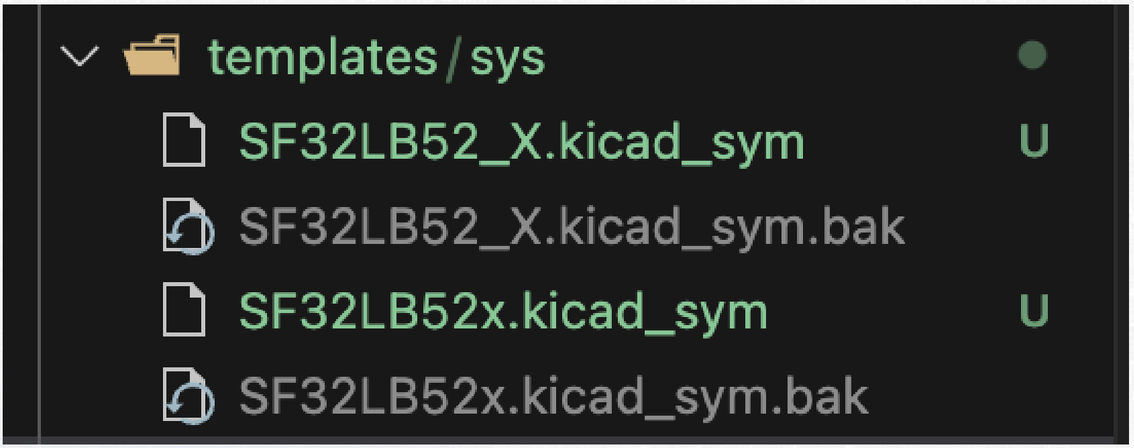


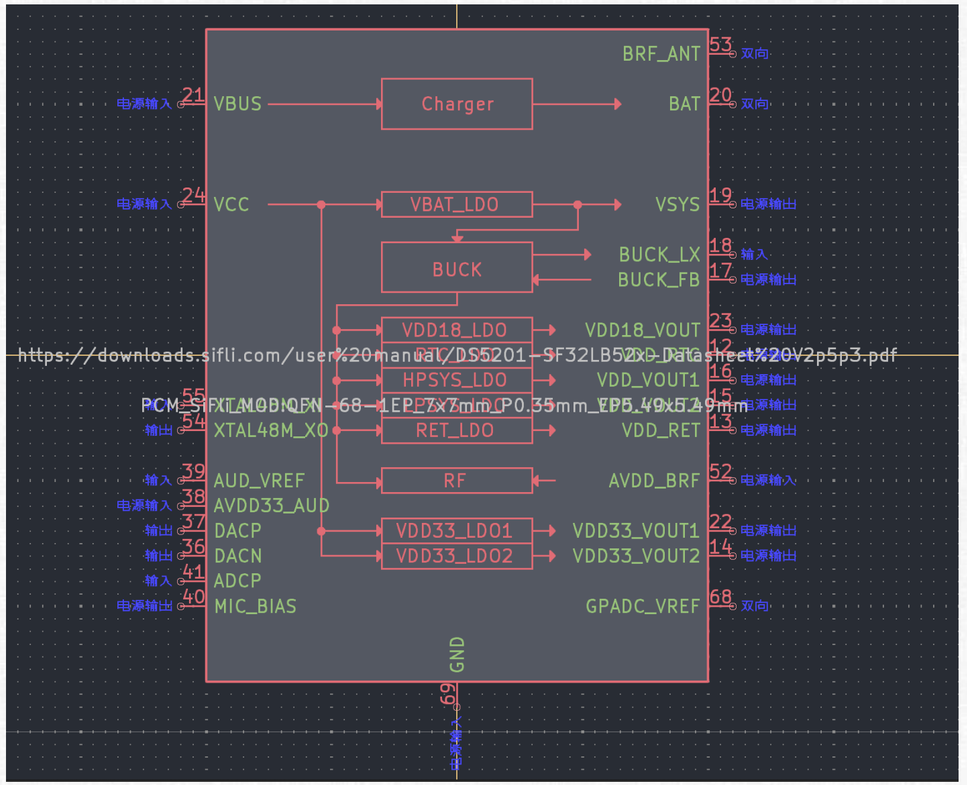


It looks awful! And it's really inconvenient for wiring in the schematic

Describe using structured data

- It is clear that the most complex parts are typically the power supply and analog sections.
- So we can manually edit this part, use it as a template, and replace it during the actual generation





Use the plugin system for release

Why do we need structured data?

- In the previous workflow, component footprints and symbols were manually created by dedicated engineers – lots of repetitive work, heavily manual, and error-prone
- Symbols may be maintained by different people, and different engineers have different tastes, so the visual style is inconsistent
- There is no effective version control mechanism, so updates are hard to propagate to every endpoint
- Software and hardware are like isolated islands, and we still have to synchronize them manually.
- The existing workflow does not adhere well to the DRY (Don’t Repeat Yourself) principle

Bridging hardware and software

- We can leverage KiCad’s plugin system to import and export alternate functions
- The alternate functions table can act as a common initialization source for various software, such as sifli-rs and Zephyr device tree
- By performing checks in the automation flow in advance, we can eliminate potential errors before actual production
- Structured data can also be used as a data source for external tools, for example tools similar to STM32CubeMX or HPMicro Tools

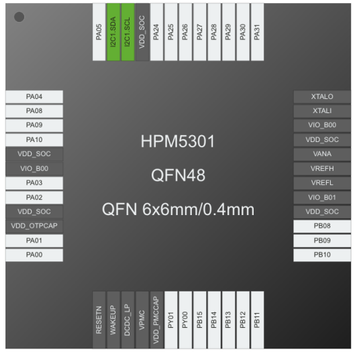
HPMicro 首页 引脚配置工具 时钟配置工具 HPM5301_QF

信号 引脚 自动组合信号 GPIOM TRGM

查询模块

- ACMP
- ADC
- EWDG
- GPIO
- GPTMR
- I2C
  - I2C0 0/2
  - I2C1 2/2
  - I2C2 0/2
  - I2C3 0/2
- JTAG
- PMIC
- SOC
- SPI
- SYSCTL
- TRGM
- UART
- USB
- USBPHY

当前函数使用引脚数: 2
配置共用引脚数: 2
复用引脚数: 0



引脚 请输入内容 删除

PinName	Signal	Loop Back	Schmitt Trigger	Pull Enable	Pull Select	Pull Resistance Strength
PA07	I2C1.SCL	Enable	N/A	Pull Enable	Pull Up	N/A
PA06	I2C1.SDA	N/A	N/A	Pull Enable	Pull Up	N/A

STM32CubeMX Untitled*: STM32H750IBKx

File Window Help myST

Home > STM32H750IBKx > Untitled – Pinout & Configuration GENERATE CODE

Pinout & Configuration | Clock Configuration | Project Manager | Tools

Software Packs Pinout

Categories A->Z

FDCAN2
FMC
I2C1
I2C2
I2C3
I2C4
LPUART1
MDIOS
QUADSPI
SDMMC1
SDMMC2
SPI1
SPI2
SPI3
SPI4
SPI5
SPI6
SWPMI1
UART4
UART5
UART7
UART8
USART1
USART2
USART3
USART6
USB_OTG_FS
USB_OTG_HS

UART4 Mode and Configuration

Mode

Mode Asynchronous
Hardware Flow Control (RS232) Disable
Hardware Flow Control (RS485)

Configuration

Reset Configuration

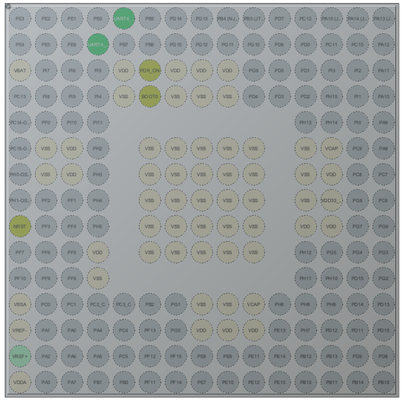
DMA Settings | GPIO Settings
User Constants | NVIC Settings
Parameter Settings

Configure the below parameters :

Search (Ctrl+F)

Basic Parameters
Baud Rate 115200 Bits/s
Word Length 8 Bits (including Parity)
Parity None

Pinout view | System view



UFBGA176 +25 (Top view)

谢谢

THANKS